IN THE CLAIMS:

1. A method of fabricating an integrated circuit comprising the steps of:

forming a HDP (high density plasma) liner layer over a semiconductor body having metal leads formed thereon, wherein a portion of said HDP liner layer over said metal leads has sloped edges;

forming a gap-fill layer over said liner layer, said gap-fill layer filling a space between closely-spaced ones of said metal leads;

forming a dielectric layer over said gap-fill layer and said metal leads; and

forming a via through said dielectric layer to at least one of said closely-spaced metal leads.

2. The method of claim 1, wherein said sloped edges have a slope on the order of 45°.

3. The method of claim 1, wherein said dielectric layer comprises PETEOS.

4. The method of claim 1, wherein said dielectric layer comprises a silane based oxide.

5. The method of claim 1, wherein the portion of HDP liner layer over the metal leads is approximately triangular shaped.

6. The method of claim 1, wherein the portion of HDP liner layer over the metal leads is approximately trapezoidal.

7. The method of claim 1, wherein said step of forming said HDP liner layer uses an etch-to-deposition ratio in the range of 0.18 to 0.40.

8. The method of claim 1, wherein said HDP liner layer comprises undoped HDP silicon dioxide.

9. The method of claim 1, wherein said HDP liner layer comprises fluorinated HDP oxide.

10. The method of claim 1, wherein said HDP liner layer comprises phosphorous doped HDP oxide.

11. The method of claim 1, wherein said gap-fill layer comprises a spin-on glass.

12. The method of claim 1, wherein said gap-fill layer comprises HSQ.

13. An integrated circuit, comprising:

a liner layer over a semiconductor body and a plurality of closely-spaced metal leads, wherein a portion of the liner layer over the metal leads has sloped edges; and

a gap-fill layer located over the liner layer and filling a space between said closely-spaced metal leads.

14. The integrated circuit of claim 13, wherein said gap-fill layer comprises HSQ.

15. The integrated circuit of claim 13, wherein said gap-fill layer comprises a spin-on glass.

16. The integrated circuit of claim 13, wherein the sloped edges have a slope on the order of 45°.

17. The integrated circuit of claim 13, wherein the portion of the liner layer over the metal leads is triangular shaped.

18. The integrated circuit of claim 13, wherein the portion of the liner layer over the metal leads is trapezoidal.